2 and 4-Bit DC-18 GHz Microstrip MEMS Distributed Phase Shifters

Joseph S. Hayden[+], Andrew Malczewski[*], Jennifer Kleber[*], Charles L. Goldsmith[*], and Gabriel M. Rebeiz[+]

[+]Radiation Laboratory, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, Michigan, 49109-2122. E-mail: metz@umich.edu, rebeiz@umich.edu.

[*]Raytheon Company, Dallas, Texas. E-mail: a-malczewski@raytheon.com, j-kleber@raytheon.com, c-goldsmith@raytheon.com.

Abstract— **Two and four-bit wideband distributed microstrip phase shifters have been developed on a 21 mil (533 μm) silicon substrate for DC-18 GHz operation. Presented here is the first demonstration of microstrip distributed MEMS transmission line (DMTL) designs, periodically loaded by MEMS varactors in series with a fixed value microstrip radial stub. The two-bit design results in a reflection coefficient less than −10 dB, an average insertion loss of −2.8 dB, and a maximum phase shift of 262° at 16 GHz. The four-bit design results in a reflection coefficient less than −9 dB, an average insertion loss of −3.0 dB, and a maximum phase shift of 333° at 16 GHz.**

I. Introduction

THE DMTL phase shifters presented here [1] consist of a high impedance line ($>$ 50 Ω) capacitively loaded by MEMS bridges [2][3] and microstrip radial stubs (Figs. 1 and 2). When the MEMS bridges are in the upstate position, the loading capacitance seen by the high impedance line is the series combination of the MEMS bridge (C_b) and the microstrip stub (C_s) and is:

$$C_l = C_s C_b/(C_s + C_b) \quad (1)$$

When a bias voltage is applied between the MEMS bridge and the high impedance line using a 120 KΩ resistor, the MEMS bridge capacitance increases by a factor of 80 and the loading to the line therefore becomes dominated by the microstrip stub alone.

Microstrip stubs are a particularly beautiful aspect of these designs as the fabrication process for the stubs is extremely simple compared to a typical MIM-IM capacitor process. In addition, the stubs provide a virtual ground connection and therefore a complicated via hole process is not required. At higher frequencies ($\geq$ 30 GHz) the inductance of a via hole would present a design challenge.

The phase shift of the slow-wave structure is calculated to be:

$$\Delta\phi = \frac{\omega Z_o \sqrt{\epsilon_{r,eff}}}{c}\left(\frac{1}{Z_{lu}} - \frac{1}{Z_{ld}}\right) \quad \text{rad/m}$$

where Z_{lu} and Z_{ld} are the distributed DMTL loaded impedances, Z_o is the characteristic impedance of the high impedance microstrip line, and $c/\sqrt{\epsilon_{r,eff}}$ is the high impedance line guided velocity.

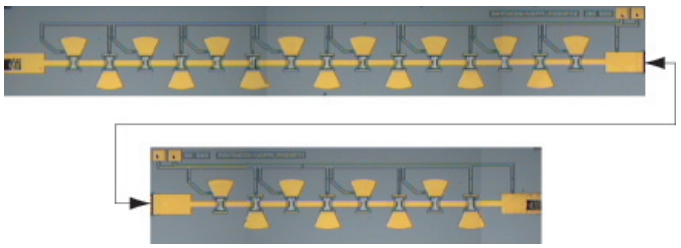

Fig. 1. Photograph of the complete 2-bit phase shifter, the 180° section is on top and the 90° section is on bottom. The sections, although normally connected, are shown here as separate parts for clarity.

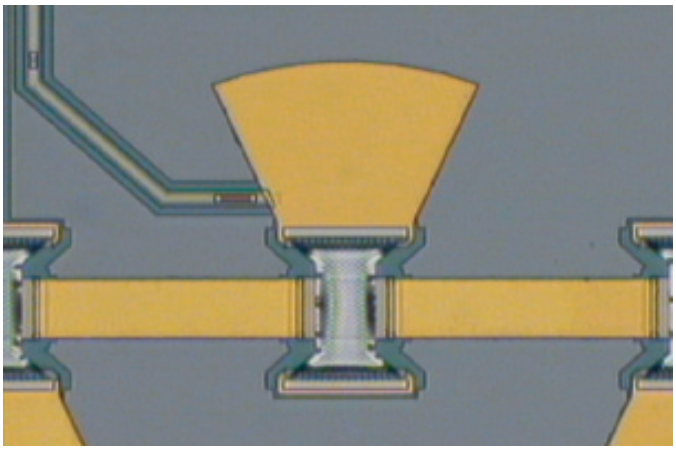

Fig. 2. Photograph of a single MEMS section. The radial stub is fed by a 120 KΩ bias line. The MEMS bridge lays over the high impedance line, which runs from left to right in the photograph.

II. Design of the DMTL Phase Shifter

The high impedance line is 130 μm wide on a 21 mil silicon substrate which results in an impedance of 78 Ω. The Bragg frequency is placed at approximately 3 times the design frequency (10 GHz) for maximum phase shift linearity [5]. The Bragg frequency can be chosen to be 1.8 times the design frequency for a smaller (in length) phase shifter, because MEMS separation will decrease with Bragg frequency, but at the expense of less phase linearity up to 18 GHz.

Closed form expressions for phase shift, MEMS separation, and loading capacitance result in the design parameters contained in Table I. Modeling of the phase shifter

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TABLE I

Design parameters for the cascaded sections of the 2 and 4-bit microstrip MEMS DMTL phase shifters.

	180°	90°	45°	22.5°
sections	15	8	4	2
MEMS separation (μm)	688	688	688	688
Z_o (Ω)	78	78	78	78
$\epsilon_{r,eff}$	7.3	7.3	7.3	7.3
Z_{lu} (Ω)	63	64	64	64
Z_{ld} (Ω)	49	52	52	52
f_b (GHz)	33	35	35	35
C_s (fF)	120	99	99	99
stub length (μm)	395	360	360	360

TABLE II

Measured phase shift of the microstrip 2-bit MEMS DMTL phase shifter.

state	16 GHz
1	0°
2	−87°
3	−175°
4	−262°

is performed on HP Series IV [4] and include the high impedance line microstrip model, MEMS switch model, and radial stub microstrip model.

III. Calibration and Measurements

The DMTL microstrip phase shifters are connected using a 6 mil-long, 5 mil-wide, 0.5 mil-thick gold ribbon to off-chip alumina substrate microstrip to CPW transitions. Calibration is performed up to the probe tip ends using a load, reflect, match (LRM) standard on an alumina substrate. Measurements of the DMTL phase shifter therefore include the input and output transitions and ribbons. The effect of the transitions and ribbons are de-embedded by a linear model which removes a total (back to back) loss of −0.05 dB of insertion loss at 10 GHz and −0.2 dB at 16 GHz as well as phase shift of these transitions. The effect of the transition line on return loss cannot be easily de-embedded.

The MEMS structure is measured in a nitrogen environment following a dehydration bake cycle to reduce humidity caused sticking of the MEMS bridge to the nitride covered microstrip high impedance line underneath. Pulldown of the MEMS bridges is 40-46 V and the MEMS bridge can be maintained in the down-state position using a 15 V bias voltage.

IV. Two-bit and Four-bit Measurements

The measured performance of the two-bit phase shifter, which consists of cascaded 180° and 90° sections, is shown in Fig. 3. Return loss for the four states is < -10 dB, and average insertion loss is −2.8 dB at 16 GHz. Table II lists the measured phase shift for the four states.

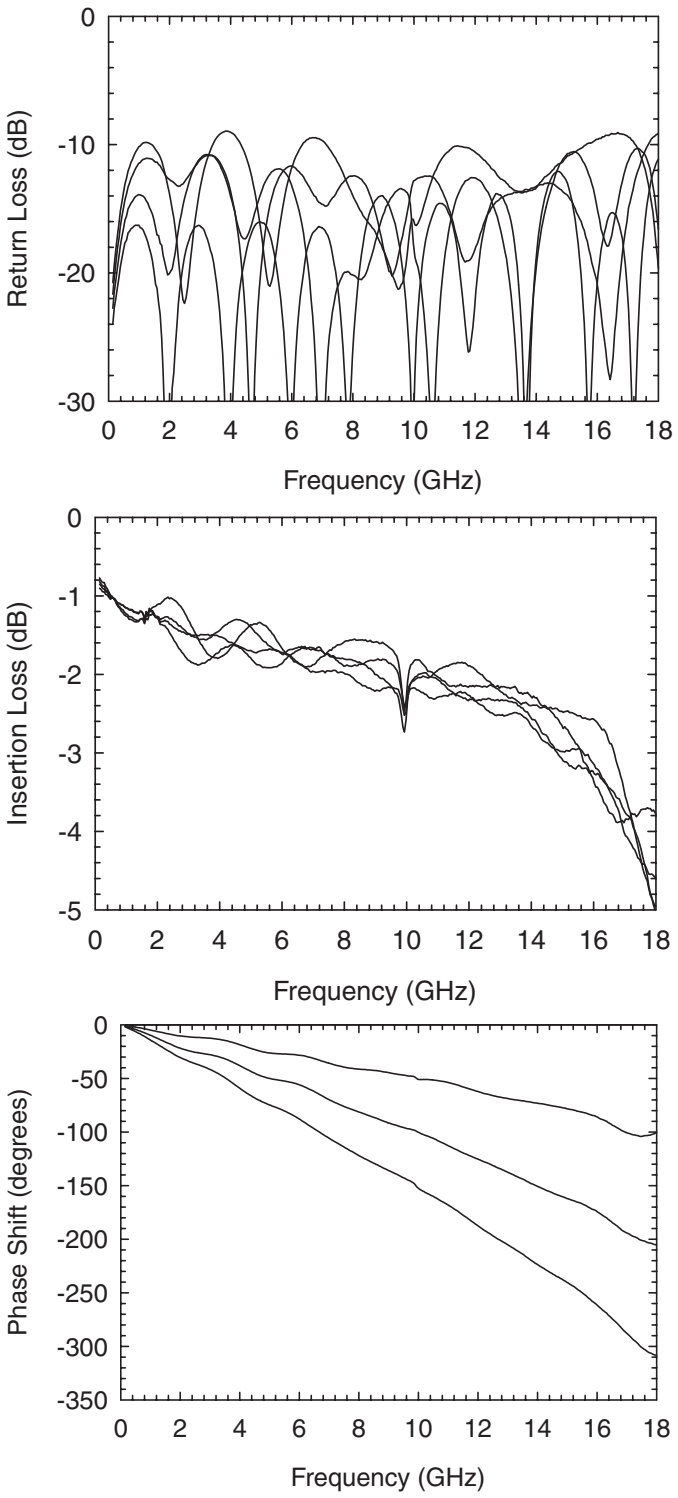

Fig. 3. Measured results of the microstrip 2-bit MEMS DMTL phase shifter.

TABLE III
MEASURED PHASE SHIFT OF THE MICROSTRIP 4-BIT MEMS DMTL PHASE SHIFTER AT 16 GHz.

state	measured	design	error
1	0°	0°	0°
2	−22°	−22.5°	+0.5°
3	−51°	−45°	−6°
4	−68.5°	−67.5°	−1°
5	−87°	−90°	+3°
6	−106°	−112.5°	+6.5°
7	−135°	−135°	0°
8	−153.5°	−157.5°	+4°
9	−180°	−180°	0°
10	−199.5°	−202.5°	+3°
11	−229°	−225°	−4°
12	−244.5°	−247.5°	+3°
13	−264°	−270°	+6°
14	−284°	−292.5°	+8.5°
15	−312°	−315°	+3°
16	−332.5°	−337.5°	+5°

TABLE IV
INSERTION LOSS CONTRIBUTIONS TO THE MICROSTRIP 4-BIT MEMS DMTL PHASE SHIFTER.

loss contribution	16 GHz
plated line sections	0.7
thin line sections	1.1
MEMS bridges	0.2
microstrip stubs	1.3
total loss	3.3
measured average loss	3.0

The measured performance of the four-bit phase shifter, which consists of cascaded 180°, 90°, 45°, and 22.5° sections is shown in Fig. 4. Return loss for the 16 states is < -9 dB, and the average insertion loss is −3.0 dB at 16 GHz. Table III lists the measured phase shift for the 16 states and as can be seen in the Table, the 4-bit phase response is accurate within +8.5/-6° of the ideal at 16 GHz.

V. Loss Contributions

There are four main contributions to the insertion loss in the DMTL phase shifter: 1) line loss of the plated high impedance line (500 μm long out of each 688 μm section), 2) line loss of the thin high impedance line under the MEMS bridge (188 μm long out of each 688 μm section), 3) bridge loss (0.5 Ω per MEMS bridge), and 4) Q loss in the microstrip radial stub (Q=85), which is extracted from measured data. Table IV contains the estimates of losses for the 4-bit phase shifter which are attributable to each of these factors.

VI. Conclusions

The microstrip DMTL MEMS phase shifters presented here are very wideband. In fact, the phase shift remains

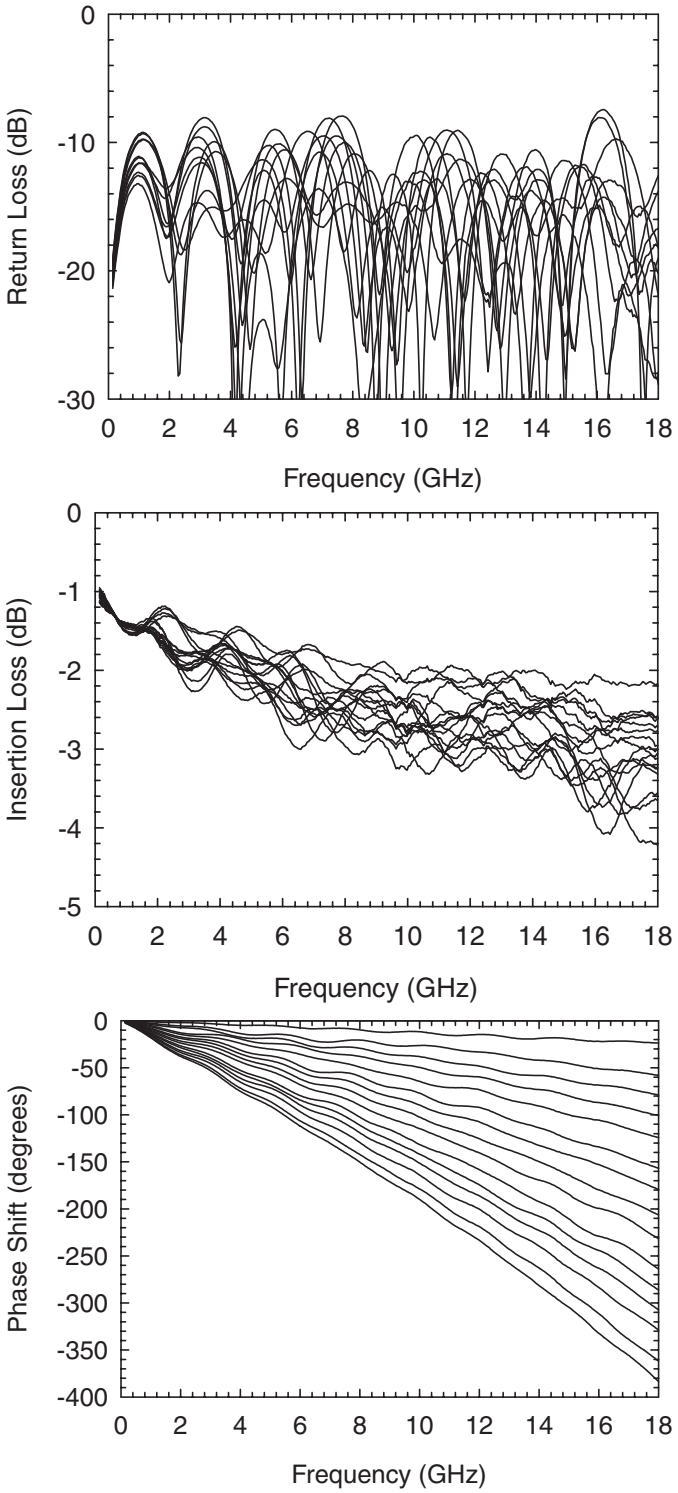

Fig. 4. Measured results of the microstrip 4-bit MEMS DMTL phase shifter.

linear up to 20 GHz even if the microstrip line becomes lossy due to radiation. This first-cut design can be optimized by lengthening the radial stubs so that the DMTL is loaded to more optimal impedances (60 and 42 Ω) for maximum phase shift and minimum reflection loss. Also, a large part of the insertion loss is due to the thin metal layer underneath the MEMS bridges. The insertion loss will improve by 0.7-0.8 dB if a thicker metal layer is used. Phase response is accurate within $+8.5/-6$ degrees at 16 GHz and in general, return loss is very reasonable at < -10 dB for DC-18 GHz.

VII. Acknowledgements

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